DATA SHEET

TDA1565TH
High efficiency 2 × 40 W / 2 Ω stereo car radio power amplifier

Product specification
2004 Jan 27
Supersedes data of 2003 Aug 13

Philips
Semiconductors

PHILIPS

High efficiency 2 × 40 W / 2 Ω stereo car radio power amplifier

TDA1565TH

FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- Differential inputs with high Common Mode Rejection Ratio (CMRR)
- Mute, standby or operating mode selectable by pin
- Load dump protection circuit
- Short-circuit safe to ground; to supply voltage and across load
- Loudspeaker protection circuit
- Thermal protection at high junction temperature
- Device switches to single-ended operation at high junction temperature
- Clip detection at 2.5 % THD
- Diagnostic signal indicating clipping, short-circuit protection and pre-warning of thermal protection.

GENERAL DESCRIPTION

The TDA1565TH is a monolithic power amplifier in a 20-lead heatsink small outline plastic package. It contains two identical 40 W amplifiers. Power dissipation is minimized by switching from SE to BTL mode only when a higher output voltage swing is needed. The device is developed primarily for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC-biased	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	8	A
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\lvert Z_i \rvert$	differential input impedance		90	120	150	kΩ
P_o	output power	R_L = 2 Ω; THD 0.5 %	25	31	–	W
		R_L = 2 Ω; THD 10 %	37	40	–	W
		R_L = 2 Ω; EIAJ	–	60	–	W
G_v	voltage gain		25	26	27	dB
CMRR	common mode rejection ratio	f = 1 kHz; R_S = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R_S = 0 Ω	50	65	–	dB
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	100	mV
α_{cs}	channel separation	R_S = 0 Ω; P_o = 25 W	50	70	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1565TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-3

BLOCK DIAGRAM

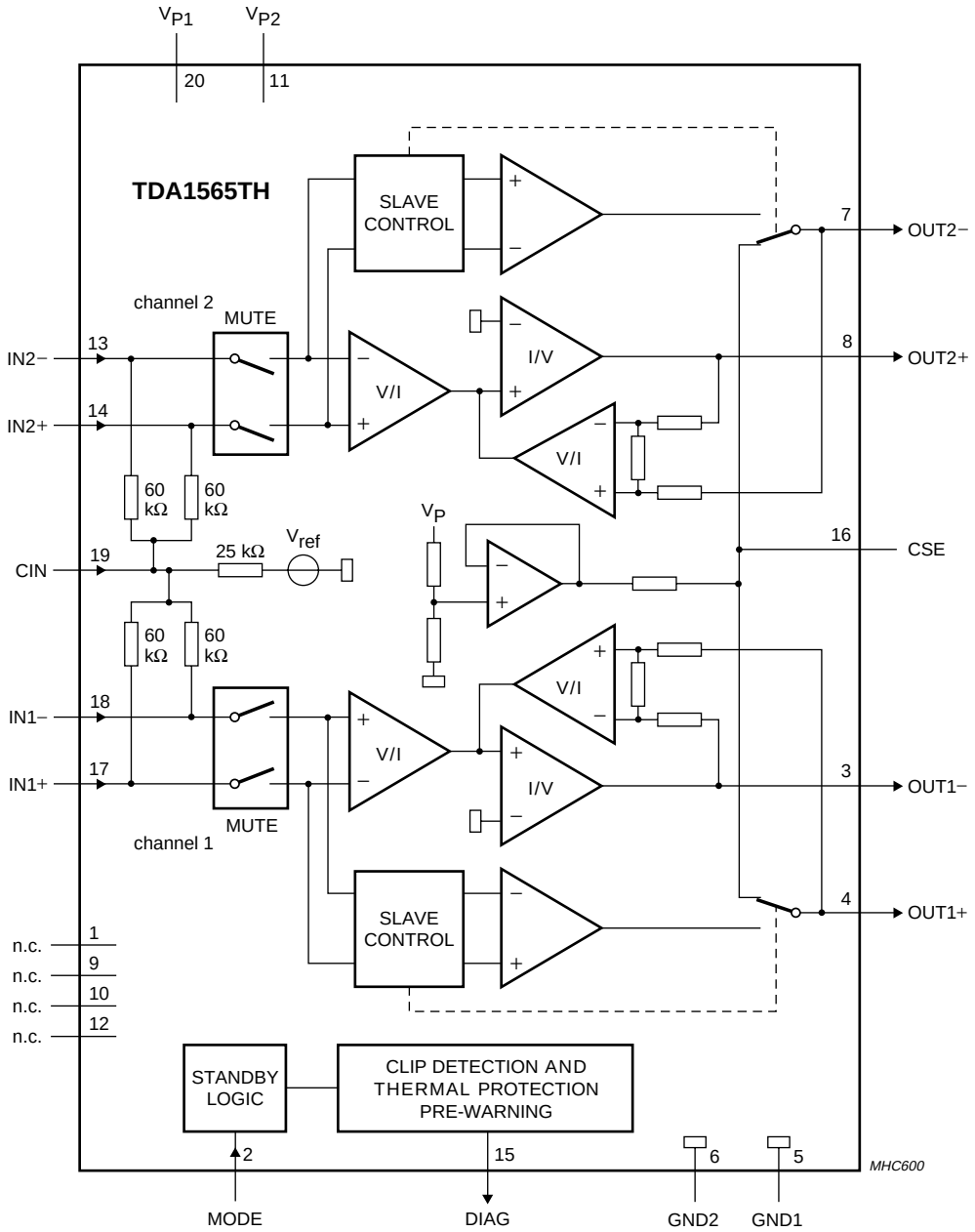


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MODE	2	mute/standby/operating mode selection
OUT1–	3	inverting channel 1 output
OUT1+	4	non-inverting channel 1 output
GND1	5	ground 1
GND2	6	ground 2
OUT2–	7	inverting channel 2 output
OUT2+	8	non-inverting channel 2 output
n.c.	9	not connected
n.c.	10	not connected
V_{P2}	11	supply voltage 2
n.c.	12	not connected
IN2–	13	inverting channel 2 input
IN2+	14	non-inverting channel 2 input
DIAG	15	diagnostic output
CSE	16	electrolytic capacitor for SE mode
IN1+	17	non-inverting channel 1 input
IN1–	18	inverting channel 1 input
CIN	19	common input
V_{P1}	20	supply voltage 1

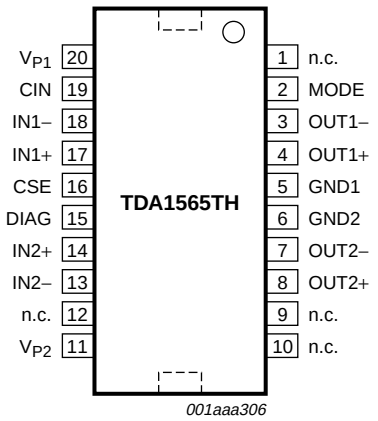


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1565TH contains two identical amplifiers with differential inputs. At low output power (output amplitudes of up to 3 V (RMS) at V_P = 14.4 V), the device operates as a normal SE amplifier. When a larger output voltage swing is required, the circuit automatically switches internally to BTL operation.

With a sine wave input signal, the power dissipation of a conventional BTL amplifier with an output power of up to 3 W is more than twice the power dissipation of the TDA1565TH (see Fig.10).

During normal use, when the amplifier is driven by typical variable signals such as music, the high (BTL) output power is only needed for a small percentage of time. Assuming that a music signal has a normal (Gaussian) amplitude distribution, the power dissipation of a conventional BTL amplifier with the same output power is approximately 70 % higher (see Fig.11).

The heatsink must be designed for music signal operation. When such a heatsink is used, the IC's thermal protection will disable the BTL mode when the junction temperature exceeds 150 °C. In this case the output power is limited to 10 W per amplifier. The gain of each amplifier is internally fixed at 26 dB.

The device can be switched to any of the following modes by applying the appropriate voltage to the MODE pin (see Fig.3):

- Standby with low standby current (less than 50 μA)
- Mute condition; DC adjusted
- On, operation.

The device is fully protected against a short-circuit of the output pins to ground or to the supply voltage. It is also protected against a loudspeaker short-circuit and against high junction temperatures. In the event of a permanent short-circuit condition, the output stage is repeatedly switched on and off with a low duty-cycle resulting in low power dissipation.

When the supply voltage drops below 6 V (e.g. vehicle engine start), the circuit is immediately muted to prevent audible 'clicks' that may be produced in the electronic circuitry preceding the power amplifier.

The voltage across the SE electrolytic capacitor connected to pin 16 is kept at 0.5 V_P by a voltage buffer (see Fig.1). The capacitor value has an important influence on the output power in SE mode, especially at low frequency signals; a high value is recommended to minimize power dissipation at low frequencies.

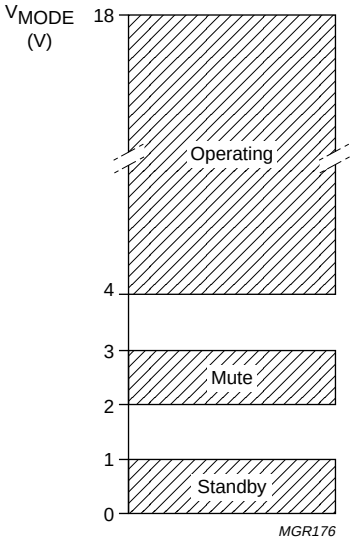


Fig.3 Switching levels of the mode select pin (pin MODE).

The diagnostic output indicates the following conditions:

- Clip detection at 2.5 % THD (see Fig.4)
- Short-circuit protection (see Fig.5):
  - When an output short-circuit occurs (for at least 10 μs); the output stages are switched off for approx. 500 ms, after which time the outputs are checked to see if a short-circuit condition still exists. During any short-circuit condition, the power dissipation is very low. During a short-circuit condition pin DIAG is at logic LOW.
- Start-up/shutdown; when the product is internally muted
- Thermal protection pre-warning:
  - If the junction temperature rises above 145 °C but is below the thermal protection temperature of 150 °C, the diagnostic output indicates that the thermal protection condition is about to become active. This pre-warning can be used by another device to reduce the amplitude of the input signal which would reduce the power dissipation. The thermal protection pre-warning is indicated by a logic LOW at pin DIAG.

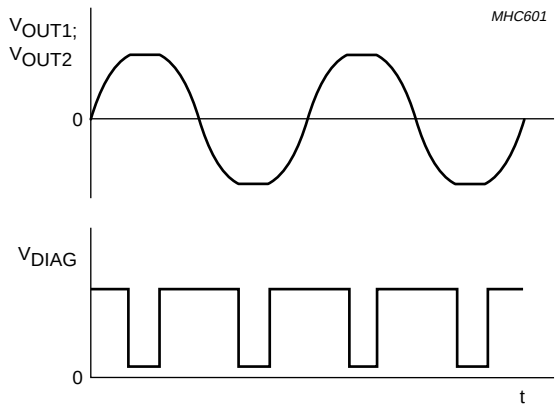


Fig.4 Clip detection waveforms.

Heatsink design

There are two parameters that determine the size of the heatsink. The first is the rating of the virtual junction temperature and the second is the ambient temperature at which the amplifier must still deliver its full power in the BTL mode.

Example:

With a conventional BTL amplifier, the maximum power dissipation for a typical signal, such as music (at each amplifier) will be approximately two times 15 W. At a virtual junction temperature of 150 °C and a maximum ambient temperature of 65 °C, $R_{th(vj-c)}$ = 1.8 K/W and $R_{th(c-h)}$ = 0.2 K/W. For a conventional BTL amplifier the thermal resistance of the heatsink should be:

$$\frac{150-65}{2\times 15} - 1.8 - 0.2 = 0.83 \text{ K/W}$$

Compared to a conventional BTL amplifier, the TDA1565TH has a higher efficiency. The thermal resistance of the heatsink should be:

$$\frac{150-65}{2\times 10} - 1.8 - 0.2 = 2.25 \text{ K/W}$$ (see Fig.6).

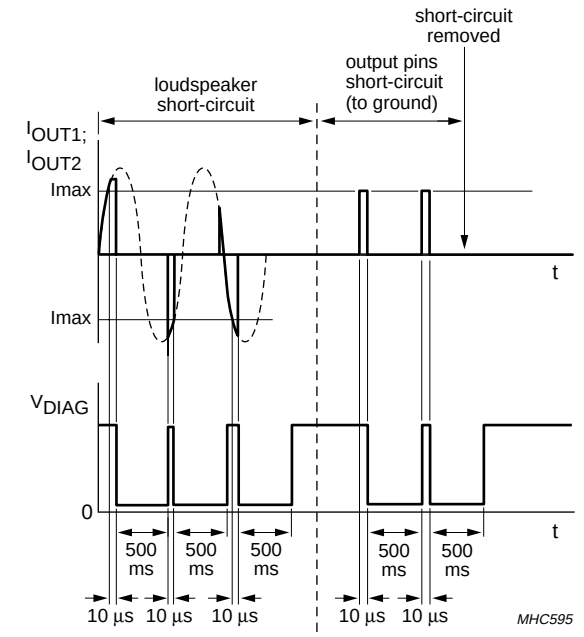


Fig.5 Short-circuit protection waveforms.

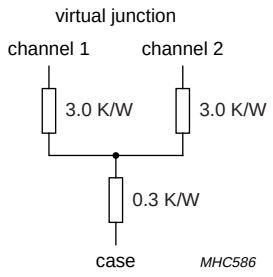


Fig.6 Equivalent thermal resistance network.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		non operating	–	30	V
		load dump; t_r > 2.5 ms	–	45	V
$V_{P(sc)}$	short-circuit safe voltage		–	16	V
V_{rp}	reverse polarity voltage		–	6	V
I_{ORM}	repetitive peak output current		–	8	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	see Fig.6	1.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(tot)}$	quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
V_{CSE}	average voltage of SE electrolytic capacitor at pin 16		–	7.1	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage	on state	–	–	100	mV
		mute state	–	–	100	mV
Mode select switch (see Fig.3)						
V_{MODE}	voltage at mode select pin	standby condition	0	–	1	V
		mute condition	2	–	3	V
		on condition	4	5	V_P	V
I_{MODE}	mode select input current	V_{MODE} = 5 V	–	25	40	μA
Diagnostic						
V_{DIAG}	voltage at diagnostic output pin	protection/temp pre-warning/clip detection	–	–	0.5	V
I_{DIAG}	diagnostic sink current	V_{DIAG} < 0.5 V	2	–	–	mA
Protection						
T_{pre}	pre-warning temperature		–	145	–	°C
$T_{dis(BTL)}$	BTL disable temperature	note 2	–	150	–	°C

Notes

1. The circuit is DC-biased at V_P = 6 to 18 V and AC-operating at V_P = 8 to 18 V.
2. If the junction temperature exceeds 150 °C, the output power is limited to 10 W per channel.

AC CHARACTERISTICS

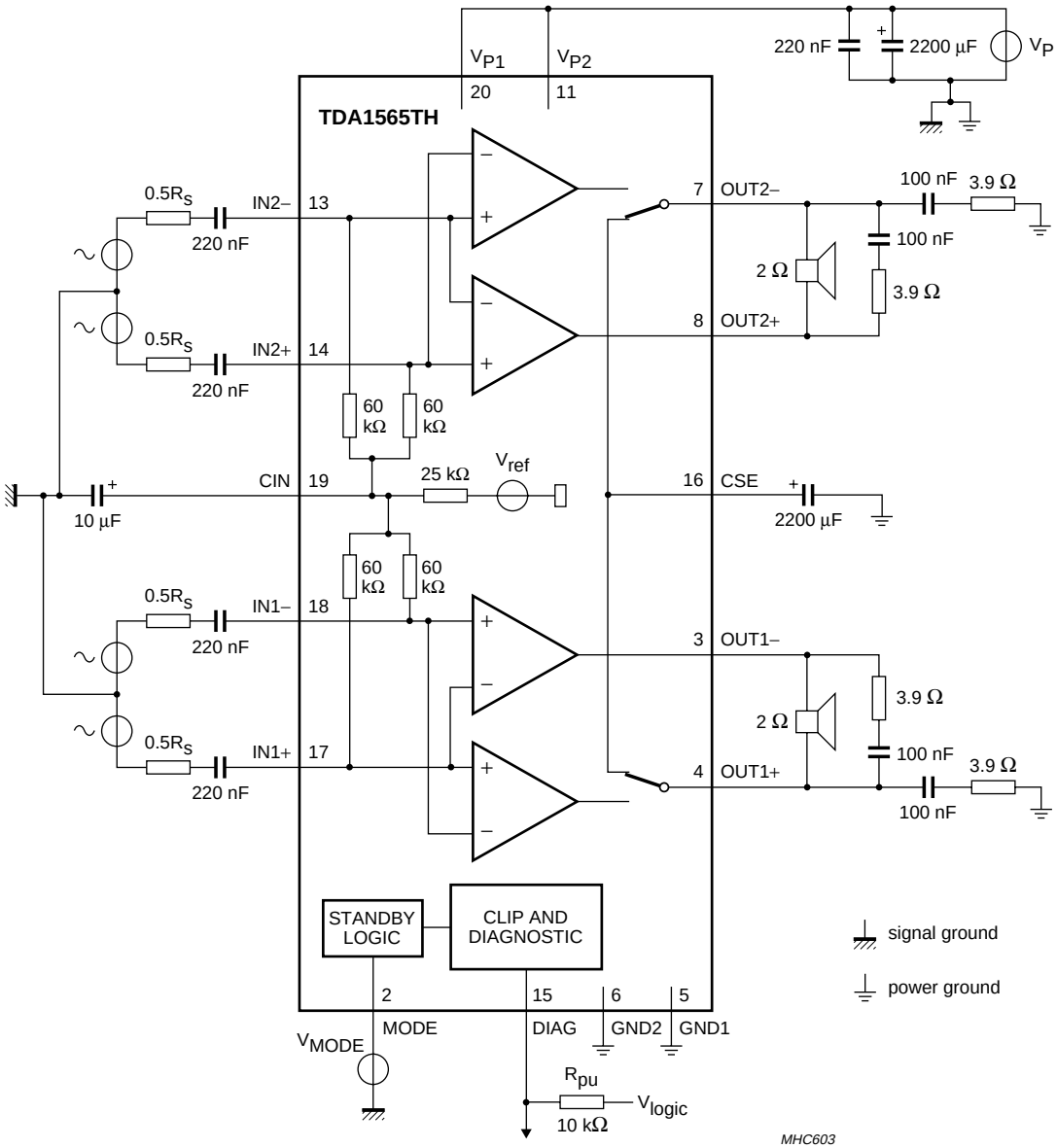
V_P = 14.4 V; R_L = 2 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	R_L = 2 Ω; THD = 0.5 %	25	31	–	W
		R_L = 2 Ω; THD = 10 %	37	40	–	W
		R_L = 2 Ω; EIAJ	–	60	–	W
		V_P = 13.2 V; THD = 0.5 %	–	26	–	W
		V_P = 13.2 V; THD = 10 %	–	34	–	W
THD	total harmonic distortion	P_o = 1 W; note 1	–	0.1	–	%
P	power dissipation		see Figs 10 and 11			W
B_p	power bandwidth	THD = 0.5 %; P_o = –1 dB with respect to 25 W	–	20 to 15000	–	Hz
$f_{ro(l)}$	low frequency roll-off	–1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	130	–	–	kHz
G_v	closed-loop voltage gain	P_o = 1 W; (see Fig.16)	25	26	27	dB
SVRR	supply voltage ripple rejection	R_S = 0 Ω; V_{ripple} = 2 $V_{(p-p)}$; (see Fig.17)				
		on/mute	50	65	–	dB
		standby		90	–	dB
CMRR	common mode rejection ratio	f = 1 kHz; R_S = 0 Ω	–	80	–	dB
$\lvert Z_i \rvert$	differential input impedance		90	120	150	kΩ
$\lvert \Delta Z_i \rvert$	mismatch in input impedance		–	1	–	%
V_{SE-BTL}	SE to BTL switch voltage level	note 3	–	3	–	V
$\lvert V_{out} \rvert$	output voltage mute (RMS value)	V_i = 1 V (RMS)	–	95	150	μV
$V_{n(o)}$	noise output voltage	on; R_S = 0 Ω; note 4	–	95	150	μV
		on; R_S = 10 kΩ; note 4	–	100	–	μV
		mute; note 5	–	90	150	μV
α_{cs}	channel separation	R_S = 0 Ω; P_o = 25 W	50	70	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

Notes

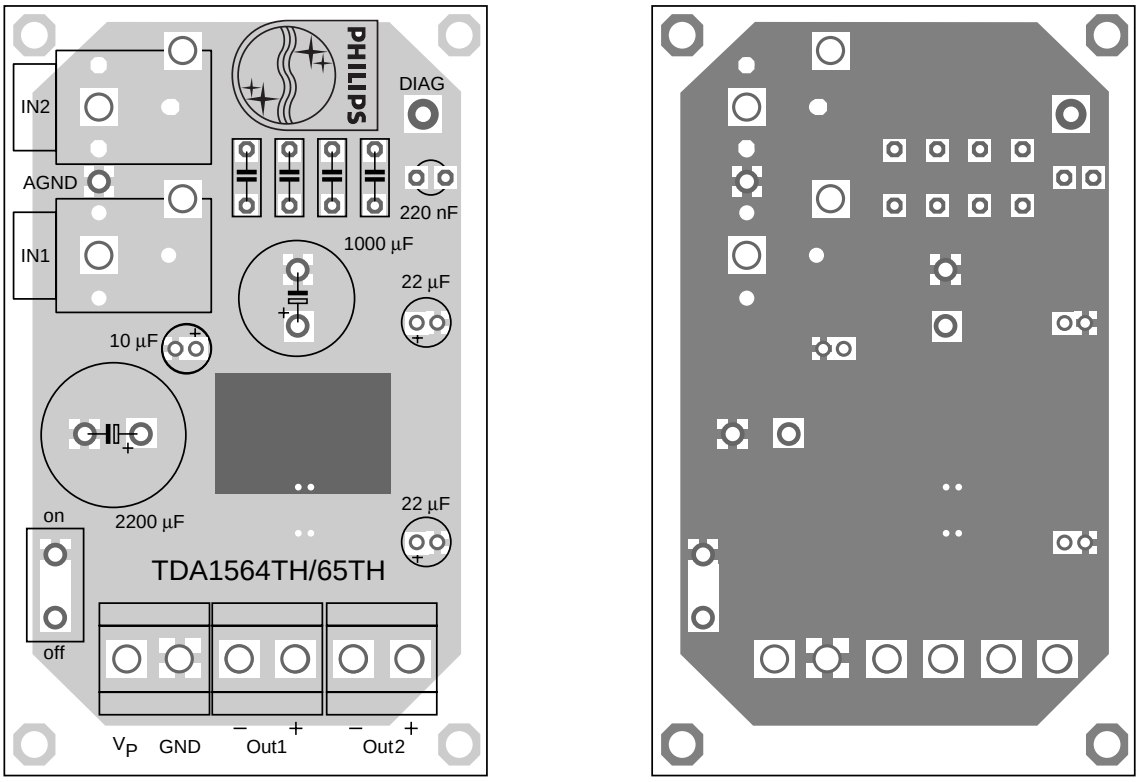
1. The distortion is measured with a bandwidth of 10 Hz to 30 kHz (see Figures 20 and 21).
2. Frequency response externally fixed (input capacitors determine the low frequency roll-off).
3. The SE to BTL switch voltage level depends on the value of V_P.
4. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage is independent of the source resistance (R_S).

TEST AND APPLICATION INFORMATION



Connect Boucherot (IEC-60268) filter to pin 4 and pin 7 using the shortest possible connection.
R_S = Source resistance.

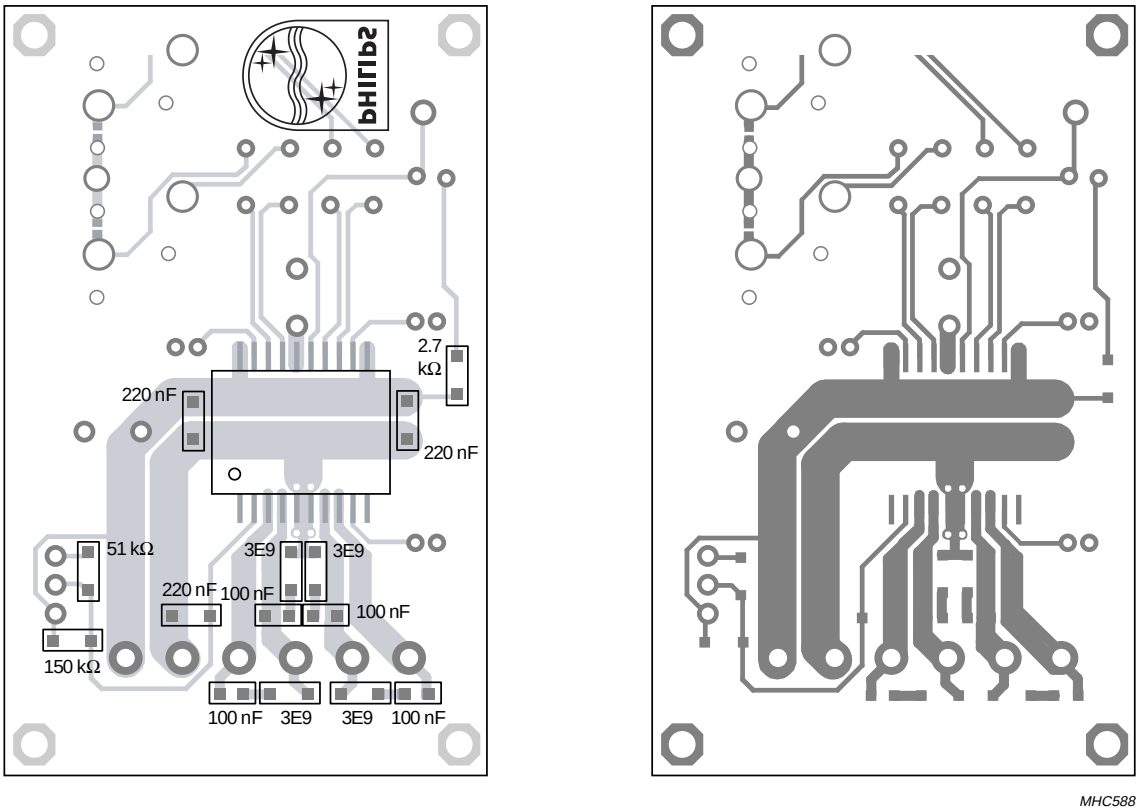
Fig.7 Application diagram.



a. Top silk screen (top view).

b. Top copper track (top view).

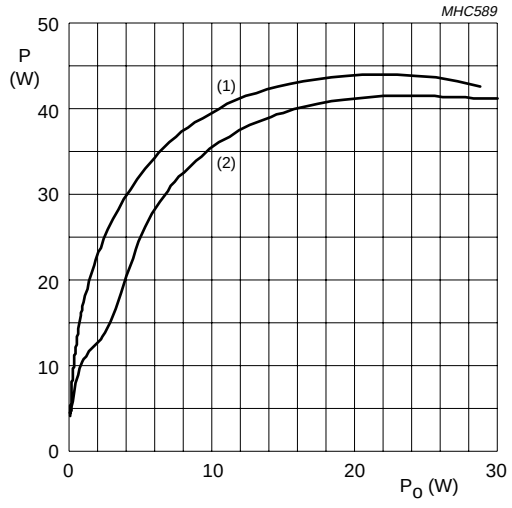
Fig.8 PCB layout (component side) for the application shown in Fig.7.



a. Bottom silk screen (top view; legend reversed).

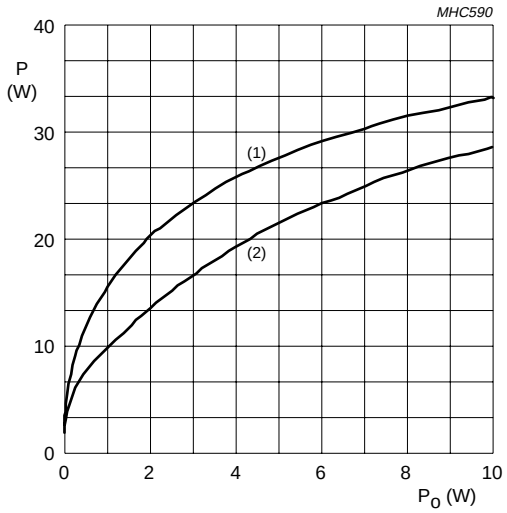
b. Bottom copper track (top view).

Fig.9 PCB layout (soldering side) for the application shown in Fig.7.



Input signal 1 kHz, sinusoidal; V_P = 14.4 V; R_L = 2 Ω.
(1) For a conventional BTL amplifier.
(2) For TDA1565TH.

Fig.10 Power dissipation as a function of output power; sine wave driven.



Input signal IEC 268 filtered pink noise; V_P = 14.4 V; R_L = 2 Ω.
(1) For a conventional BTL amplifier.
(2) For TDA1565TH.

Fig.11 Power dissipation as a function of output power; pink noise through IEC-60268 filter.

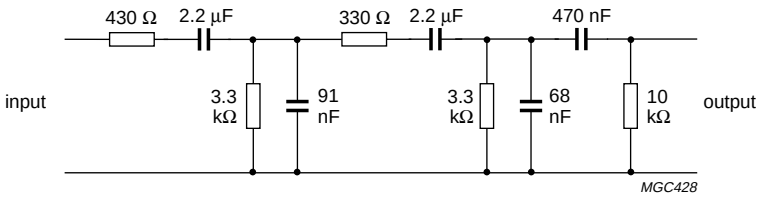


Fig.12 IEC-60268 filter.

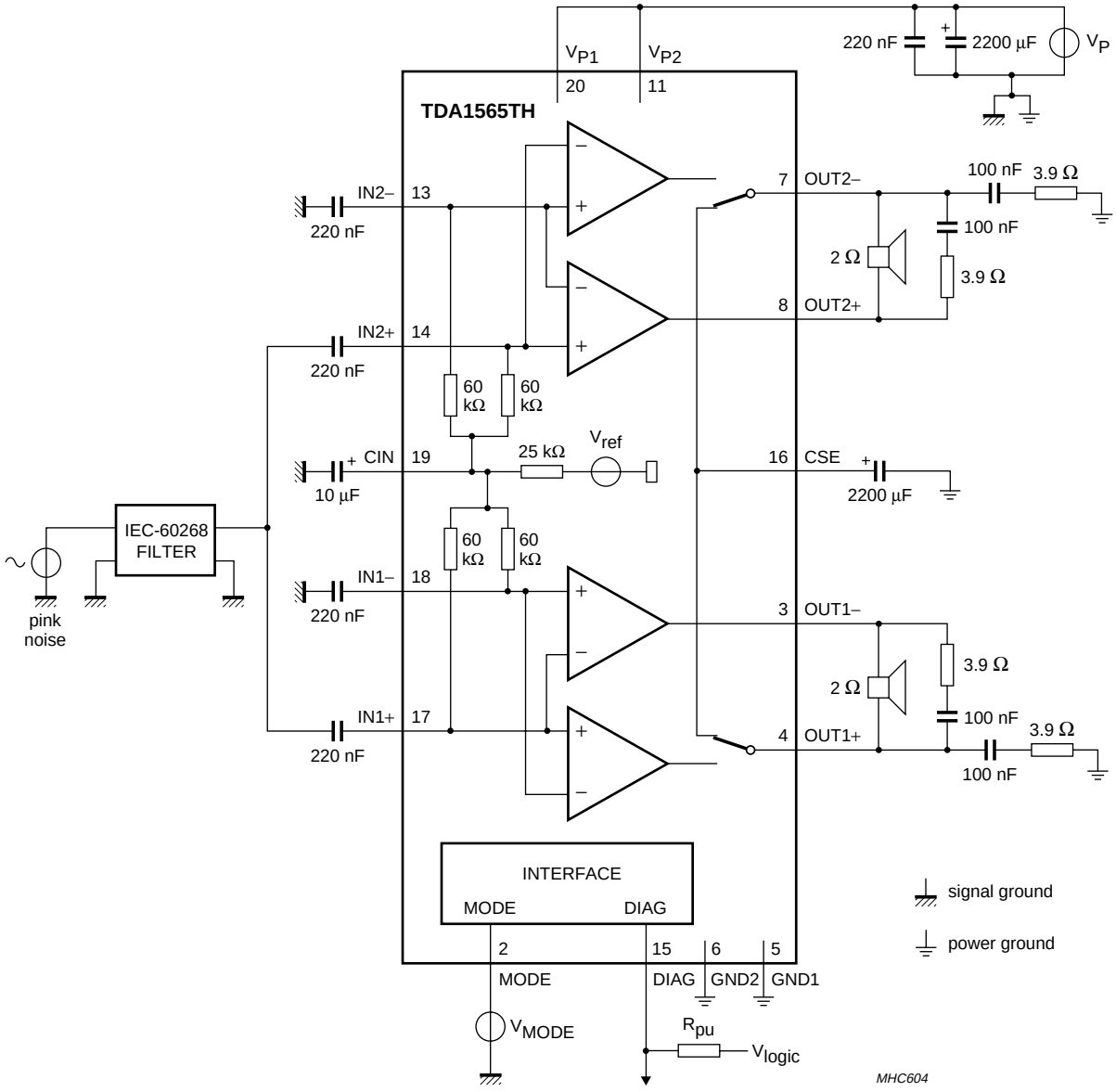
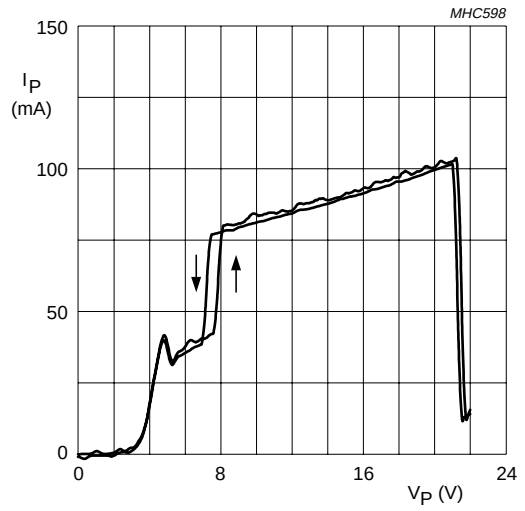
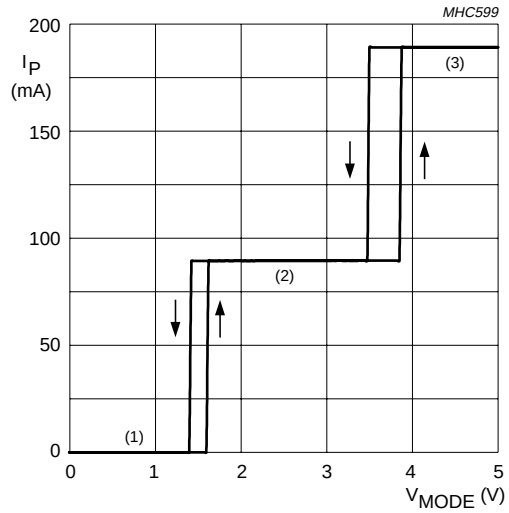


Fig.13 Test and application diagram for dissipation measurements with a simulated music signal (pink noise).



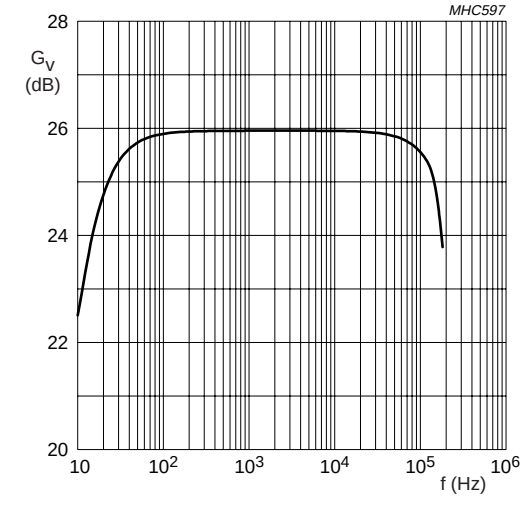
V_{MODE} = 5 V; R_L = ∞.

Fig.14 Quiescent current as a function of V_P.



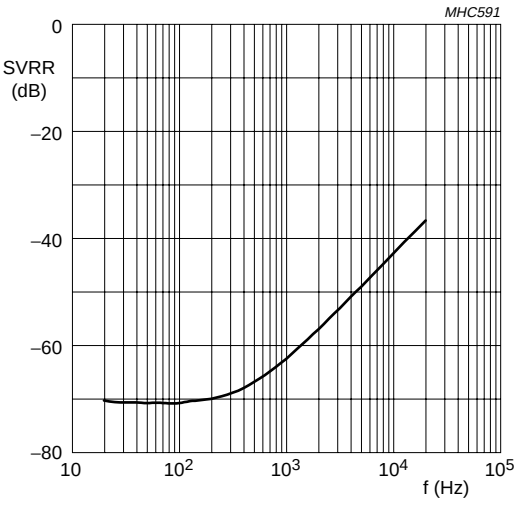
V_{IN} = 5 mV; V_P = 14.4 V.
(1) Standby.
(2) Mute.
(3) Operating.

Fig.15 I_P as a function of V_{MODE}.



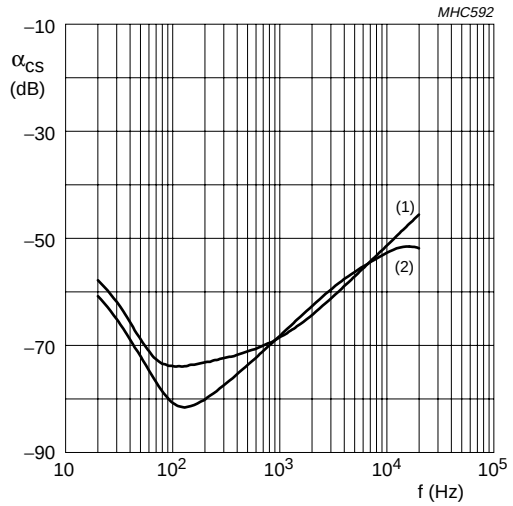
V_{IN} = 100 mV.

Fig.16 Gain as a function of frequency.



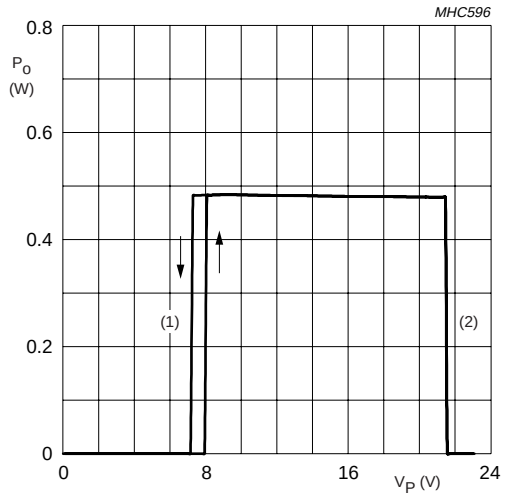
(V_{ripple} = 2 V (p-p).

Fig.17 SVRR as a function of frequency.



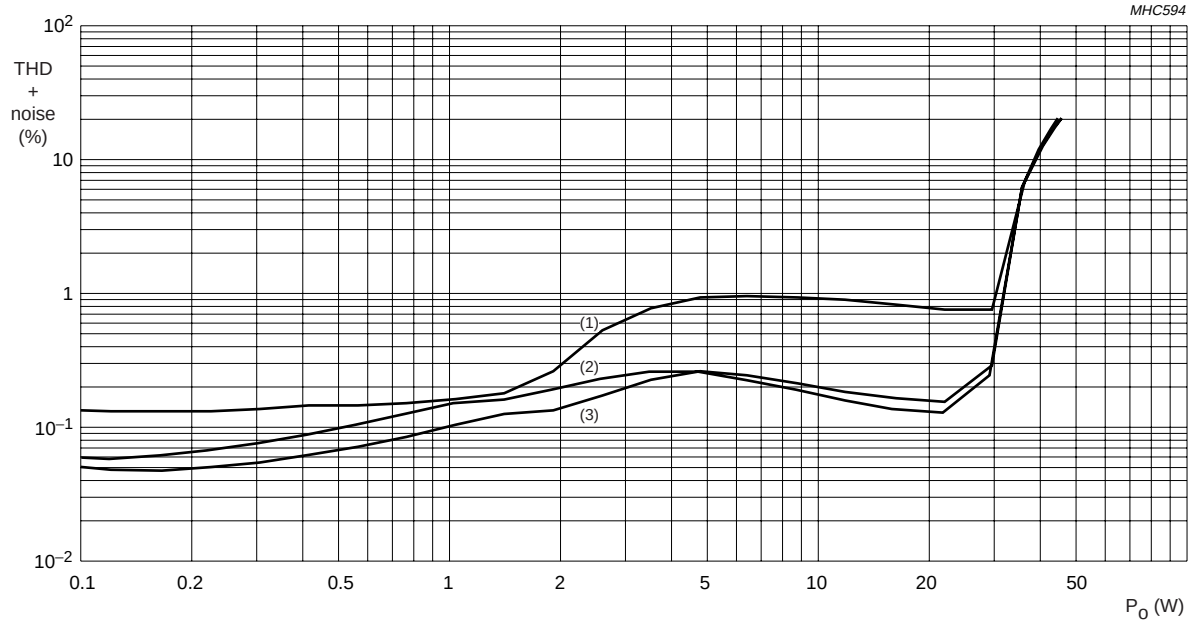
(1) P_o = 1 W.
(2) P_o = 10 W.

Fig.18 Channel separation as a function of frequency.



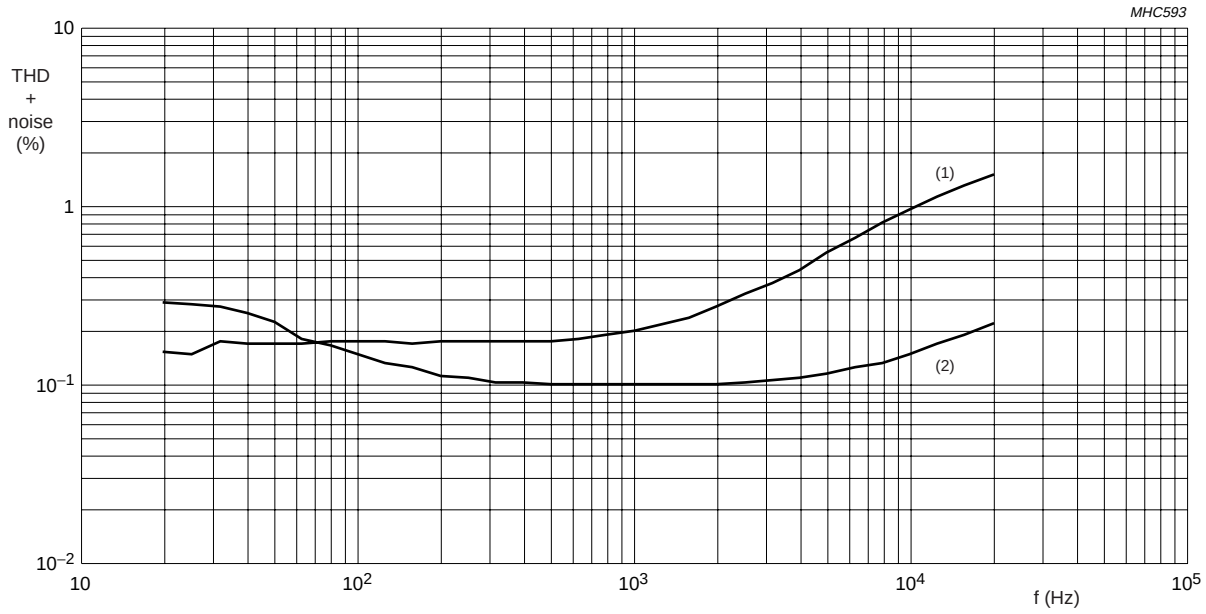
V_{IN} = 50 mV.
(1) Low supply mute.
(2) Load dump.

Fig.19 AC operation as a function of V_P.



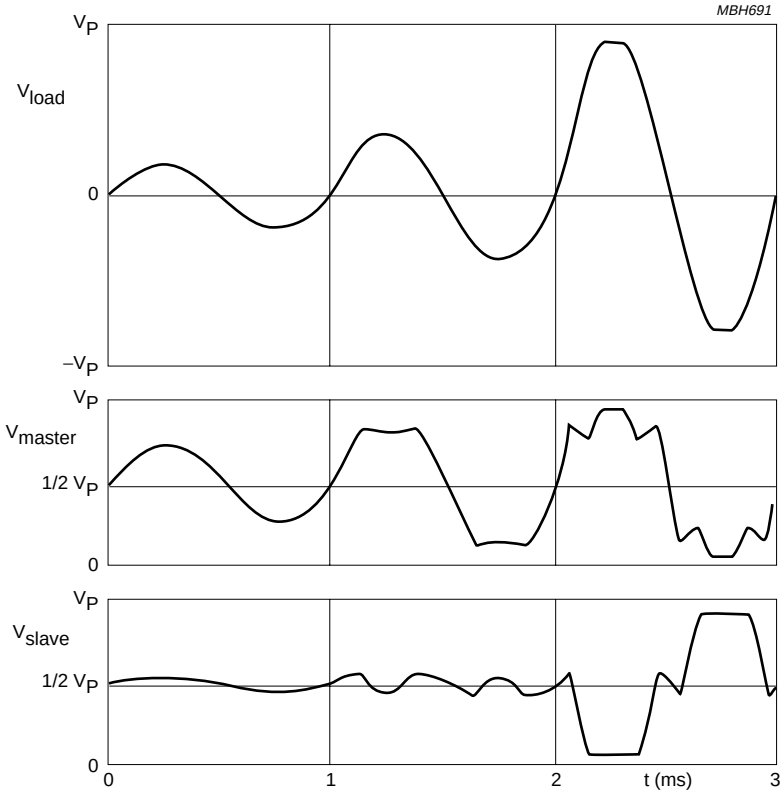
R_L = 2 Ω.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.20 THD + noise as a function of P_o.



R_L = 2 Ω.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.21 THD + noise as a function of frequency.



Also see Fig.7.
$V_{load} = (V_{OUT2+})-(V_{OUT2-})$ or $(V_{OUT1+})-(V_{OUT1-})$.
$V_{master} = V_{OUT2+}$ or V_{OUT1-}.
$V_{slave} = V_{OUT2-}$ or V_{OUT1+}.

Fig.22 Output waveforms.

Application notes

ADVANTAGES OF HIGH EFFICIENCY

1. Power conversion improvement (power supply): The fact that the reduction of power dissipation is directly related to a reduction of supply current is often neglected. One advantage is voltage is dropped over the whole supply chain. Another advantage is reduced stress for the coil in the supply line. Even the adapter or supply circuit is cooler due to the reduced dissipation of heat in the whole chain because more supply current will be converted into output power.
2. Power dissipation reduction: This is the best known advantage of high efficiency amplifiers.
3. Heatsink size reduction. The size of heatsink for a conventional amplifier can be reduced by approximately 50 % at V_P = 14.4 V when the TDA1565TH is used. In this case, the maximum heatsink temperature remains the same.
4. Heatsink temperature reduction: The power dissipation and the thermal resistance of the heatsink determine the rise in heatsink temperature.

If the same sized heatsink of a conventional amplifier is used, the maximum heatsink temperature and the maximum junction temperature both decrease, which extends the life of the semiconductor device; the maximum power dissipation for music, or similar input signals decreases by 40 %.

It is clear that the use of the TDA1565TH saves a significant amount of energy. The maximum supply current decreases by approximately 32 %, which reduces the power dissipation in the amplifier as well as in the whole supply chain. The TDA1565TH allows the size of the heatsink to be reduced by approximately 50 %, or the temperature of the heatsink to be reduced by 40 % if the size of the heatsink is unchanged.

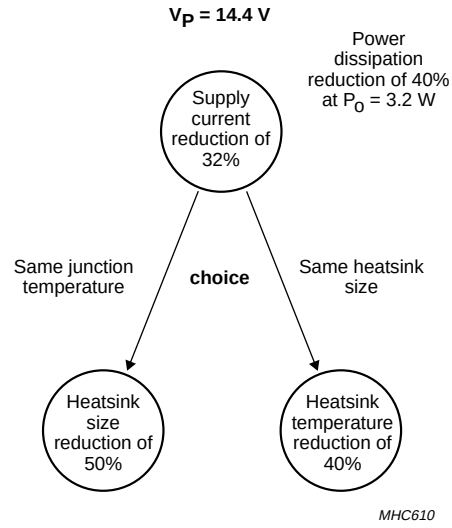
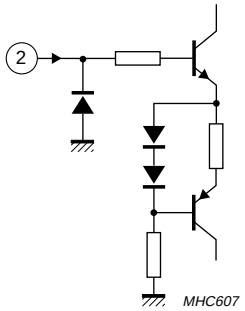
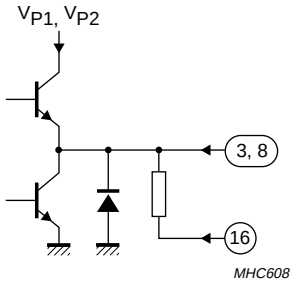
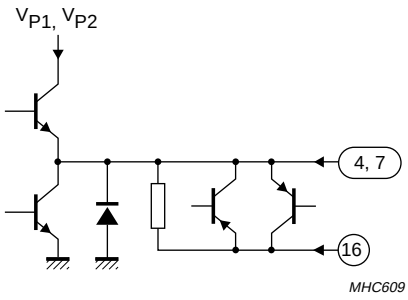
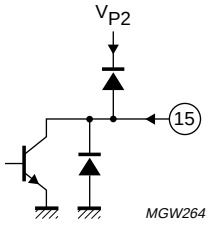


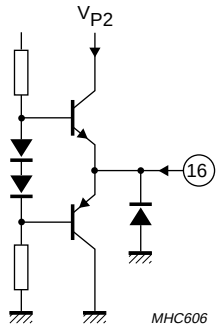
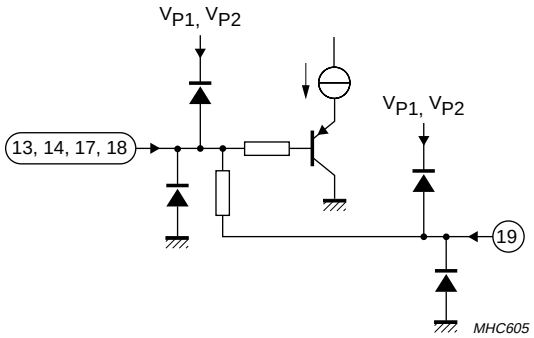
Fig.23 Heatsink design.

ADVANTAGE OF THE CONCEPT USED BY TDA1565TH

Because the TDA1565TH uses a single-ended capacitor to create a non-dissipating half supply voltage, it is highly efficient under all conditions. Other design concepts rely on the fact that both input signals have the same amplitude and phase. Using a SE capacitor prevents any adverse affects on efficiency that could result from any form of processing that may have been applied to the input signals, such as amplitude difference, phase shift or delays between both input signals, or other DSP processing.

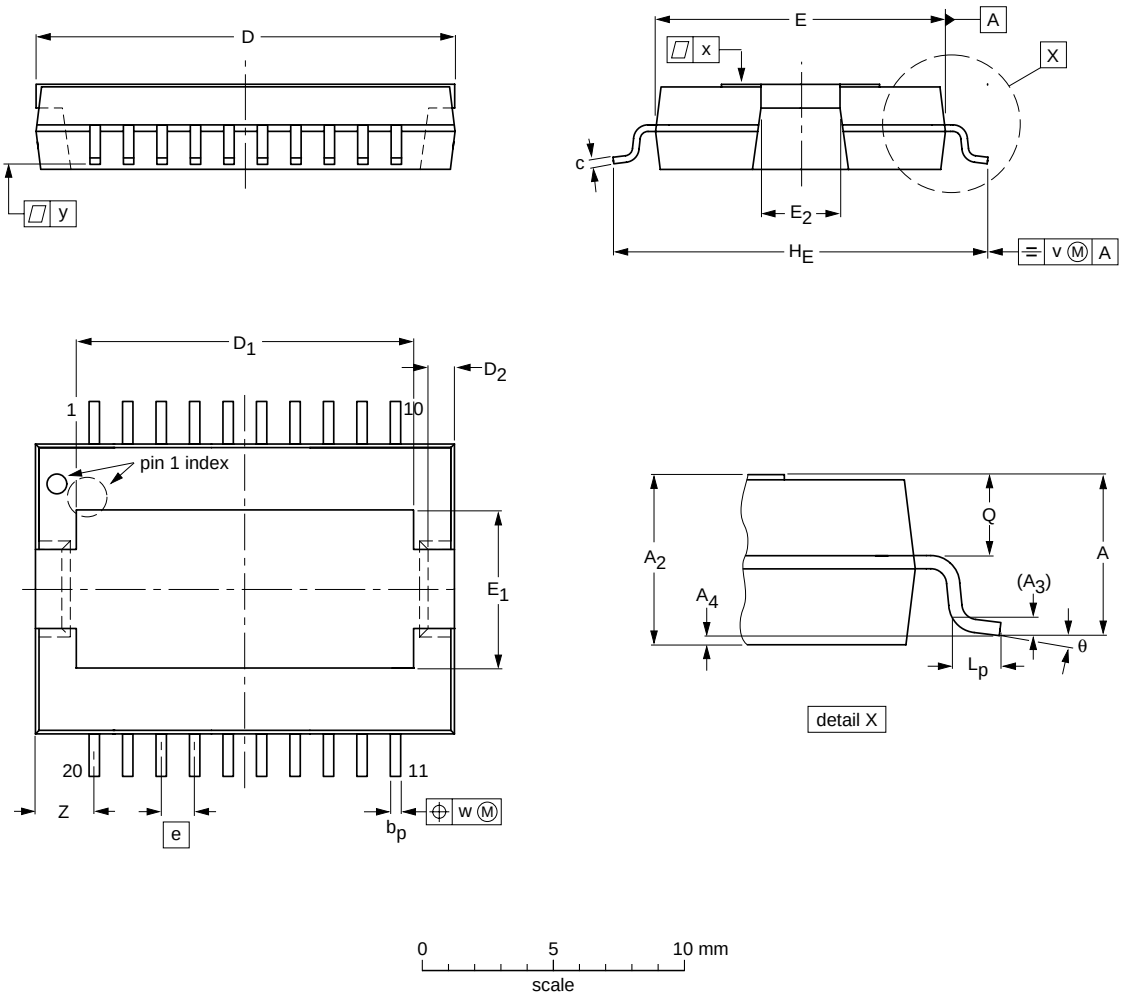
INTERNAL PIN CONFIGURATIONS

PIN	NAME	EQUIVALENT CIRCUIT
2	MODE	
3, 8	OUT1+, OUT2–	
4, 7	OUT1+, OUT2–	
15	DIAG	

PIN	NAME	EQUIVALENT CIRCUIT
16	CSE	
17, 18, 13, 14, 19	IN1+, IN1– IN2+, IN2– CIN	

PACKAGE OUTLINE

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT418-3						~~02-02-12~~ 03-07-23

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

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